REMARKS

Favorable reconsideration of this application, as presently amended and in view of the following discussion, is respectfully requested.

Claims 8-14 are pending and are presently amended. The amendments to the claims are made to correct minor idioms resulting from the translation of the application to English and to avoid interpretation under 35 U.S.C. §112, sixth paragraph. The amendments are not made in response to any rejection in the outstanding Office Action.

Applicants first wish to point out that the outstanding Office Action fails to include an initialed copy of the Form PTO-1449, filed July 23, 2001. This application had previously been allowed by the Examiner and a Request for Continued Examination was filed in order to have the references listed in the Form PTO-1449 considered. Applicants respectfully request that the Examiner provide an initialed copy of the Form PTO-1449 with the next Office communication in order to show that the cited references were fully considered by the Examiner.

In the outstanding Office Action, Claims 8-10 were rejected under 35 U.S.C. §103(a) as being unpatentable over Haghiri-Tehrani in view of Fjelstad, and Claims 8 and 10 were rejected under 35 U.S.C. §103(a) as being unpatentable over Hiroyuki in view of Fjelstad.

Attention is first directed to the rejection of Claims 8-10 over Haghiri-Tehrani in view of Fjelstad. The outstanding Office Action states that "Haghiri-Tehrani fails to disclose forming a plurality of sets of die bond and wire [b]ond pads[,] formation of a plurality of discrete semiconductor elements[,] and dividing the sealing resin into discrete semiconductor devices by cutting off the sealing resin around the discrete semiconductor devices." In

contrast, the invention of Claim 8 incorporates those missing elements to provide various advantages, including reduction of production time and costs.[1]

The Haghiri-Tehrani reference shows how an integrated circuit 22 can be incorporated on an identity card. The integrated circuit 22 is glued into a recess 32, and conductive connections 36 are then produced between the integrated circuit 22 and the contact surfaces 15-20 on the ID card.[2] In the Example provided by the Haghiri-Tehrani reference, the conductive connections 36 are bonding wires or, alternatively, a metal spider or conductive contact bumps located on the integrated circuit. In contrast, a purpose of the present invention is to avoid the use of conventional connective elements, such as bumps, to achieve greater heat dissipation and other advantages.[3] As recited in Claim 8, plural sets of die bond pads and wire bond pads are formed by fastening metal sheets at specified positions on the back of an insulating sheet and fastening the back of the discrete semiconductor elements on the die bond pads and electrically connecting the electrodes of the discrete semiconductor elements and the wire bond pads. An example of the resulting structure is shown in Figure 3 of the present application.

On the other hand, the ID cards described in Haghiri-Tehrani connect the IC 22 to the contact surfaces 15-20 of the ID card without the use of the die bond and wire bond pads defined by Claim 8. This feature of Claim 8 is also nowhere to be found in the Fjelstad reference, which was applied in the outstanding Office Action as teaching how individual packaged chips are separated from each other.[4]

---

[1]Specification, page 8, lines 12-16.

[2]Column 3, lines 27-30; column 4, lines 27-32; Figures 1, 6, and 7.

[3]Specification, page 5, lines 1-12.

[4]*See, e.g.*, column 5, lines 10-11, of the Fjelstad patent.

Thus, it can be appreciated that the Haghiri-Tehrani and Fjelstad references, when applied alone or in any proper combination, fail to teach or suggest the invention of Claim 8. More specifically, the combination of references fails to teach or suggest the claimed step of "forming a plurality of sets of die bond pads and wire bond pads by fastening electrically conductive metal sheets at specified positions on the back of an insulating sheet and making apertures in the insulating sheet on the metal sheets, [and] fastening the back of the discrete semiconductor elements on the die bond pads and electrically connecting the electrodes of the discrete semiconductor elements and the wire bond pads," as recited in Claim 8.

Moreover, it would not have been obvious to one of ordinary skill in the art to combine the Haghiri-Tehrani and Fjelstad references because their respective teachings apply to different products that are not compatible with one another. Specifically, the Haghiri-Tehrani reference shows how a single IC is connected to contact surfaces on an ID card. It would not make any sense to modify Haghiri-Tehrani to include the step of separating individual package chips because such separation would require destroying the ID card and because the ICs 22 are applied to the ID cards one at a time. Moreover, there is no advantage to modifying Haghiri-Tehrani to include multiple packaged chips on a sacrificial layer, as taught by Fjelstad. Put simply, the ID card in the Haghiri-Tehrani patent cannot be treated as a sacrificial layer 100, which is cut up in the Fjelstad patent.

Attention is now directed to the rejection of Claims 8 and 10 over Hiroyuki in view of Fjelstad[5]. It is first pointed out that the Hiroyuki reference uses inner leads 6, which are

---

[5]The outstanding Office Action cites to Hiroyuki as though the reference includes at least eleven pages. Since the Hiroyuki reference is a Japanese language document with only six numbered pages, the citations in the outstanding Office Action presumably are either incorrect or refer to a translation that was inadvertently not furnished to the Applicants. If such a translation is being relied upon to reject the claims, Applicants respectfully request a copy thereof.

largely internal to the housing 5 and protrude to form external electrodes 8. This is completely different from the invention of Claim 8, which includes the steps of "forming a plurality of sets of die bond pads and wire bond pads by fastening electrically conductive metal sheets at specified positions on the back of an insulating sheet and making apertures in the insulating sheet on the metal sheets, [and] fastening the back of the discrete semiconductor elements on the die bond pads and electrically connecting the electrodes of the discrete semiconductor elements and the wire bond pads." Figure 7B of Hiroyuki (referenced in the outstanding Office Action) shows a side view of an outer connecting wire 11, which is more clearly seen in Figure 5D. Figure 5D makes clear that the element 11 in Figure 7B is not a wire bond pad but is simply a lead wire for connecting the semiconductor device. Moreover, Figure 7B does not show both die bond pads and wire bond pads formed by fastening electrically conductive metal sheets at specified positions on the back of an insulating sheet, as required by Claim 8. Clearly, the device shown in the Hiroyuki reference neither teaches nor suggests the invention of Claim 8. The deficiencies of the Hiroyuki reference are not alleviated by the Fjelstad reference, which was applied for the mere purpose of showing that individual packaged chips may be separated from each other. Accordingly, neither Hiroyuki nor Fjelstad, when considered alone or in proper combination, anticipate or make obvious the invention of Claim 8. Moreover, there is no motivation for combining the Hiroyuki and Fjelstad references, and, in fact, based on the figures of the Hiroyuki reference, there would be no reasonable expectation of success in combining their respective teachings to arrive at the claimed invention.

Therefore, Applicants respectfully submit that Claim 8 patentably distinguishes over the references applied in the outstanding Office Action. Since Claims 9 and 10 depend from

Claim 8, Applicants also submit that Claims 9 and 10 patentably distinguish over the applied references for at least the same reasons as Claim 8.

In view of the foregoing discussion, no further issues are believed to be outstanding in the present application. Therefore, Applicants respectfully request that the present application be allowed and be passed to Issue.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Gregory J. Maier
Attorney of Record
Registration No. 25,599
Robert C. Mattson
Registration No. 42,850

22850

(703) 413-3000
Fax #: (703)413-2220
GJM/RCM/js
I:\atty\RCM\Prosecution\0057\198778.am1.wpd

Marked-Up Copy
Serial No: 09/695,311
Amendment Filed on:
3-4-02

IN THE CLAIMS

--8. (Amended) A method for producing [a] discrete semiconductor [device] devices, comprising the steps of:

forming [the] a plurality of sets of die bond [pad] pads and wire bond pads by fastening electrically conductive metal sheets at specified positions on the back of an insulating sheet and making apertures in the insulating sheet on the metal sheets,

packaging [for] the discrete semiconductor elements, said packaging step comprising fastening the back of the discrete semiconductor elements on the die bond pads and electrically connecting the electrodes of the discrete semiconductor elements and the wire bond pads,

sealing the plurality of [the] discrete semiconductor elements installed on the insulating sheet with an integral sealing resin by sealing the packaging surface of the insulating sheet with the resin, and

dividing the sealing resin into the discrete semiconductor devices by cutting off the sealing resin around the discrete semiconductor elements.

9. (Amended) A method as claimed in claim 8, wherein

the step of packaging [described above also include a step of] further comprises fastening [the] a back side electrode of the discrete semiconductor device onto the corresponding die bond pad to electrically connect the die bond pad and the back side electrode.

10. (Amended) A method as claimed in claim 8, wherein

the dividing step [also be a step of] comprises cutting off the sealing resin around a plurality of discrete semiconductor elements grouped as a single body[, to obtain] such that at least one of the discrete semiconductor [device] devices [wherein the] comprises a plurality of the discrete semiconductor elements [are] sealed with the integral resin.

11. (Amended) A method for producing a discrete semiconductor device, comprising the steps of:

packaging [step wherein] a plurality of discrete semiconductor elements [are fastened, on], said packaging step comprising fastening the back [thereof,] of the discrete semiconductor elements onto an electrically conductive metal sheet and connecting electrically an electrode of each discrete semiconductor element [is electrically connected] to a specified position of the metal sheet,

sealing the packaging surface of the metal sheet with an integral sealing resin,

[a cut-off step of] cutting off the metal sheet by cutting therein from the back [thereby] to turn the metal sheet into die bond pads and wire bond pads which are arranged at intervals, and

dividing the discrete semiconductor devices by cutting off the sealing resin around the discrete semiconductor elements.

12. (Amended) A method as claimed in claim 11, wherein

the packaging step [also include a step of] comprises fastening the back electrode of the discrete semiconductor elements onto the metal sheet and electrically connecting the metal sheet and the back electrode.

13. (Amended) A method as claimed in claim 11, wherein

the dividing step [also be a step of] comprises cutting off the sealing resin around a plurality of discrete semiconductor elements grouped as a single body, to divide the discrete

semiconductor devices each carrying the plurality of discrete semiconductor elements being sealed with the integral resin.

14. (Amended) A method as claimed in claim 11, wherein

the [cut-off step also be a] step of cutting off the metal sheet comprises cutting off the metal sheet[in] such that [a way as] the die bond pads and/or the wire bond pads connected to the plurality of discrete semiconductor elements become an integral body, and

the dividing step [also be a step off] comprises cutting off the sealing resin around the discrete semiconductor elements which are formed so that the die bond pads and/or the wire bond pads connected to the plurality of discrete semiconductor elements become an integral body, thereby to obtain the discrete semiconductor device wherein the plurality of discrete semiconductor elements which share the die bond pads and/or the wire bond pads in common are sealed with the integral resin.--